ACADEMIC PLANNER

For

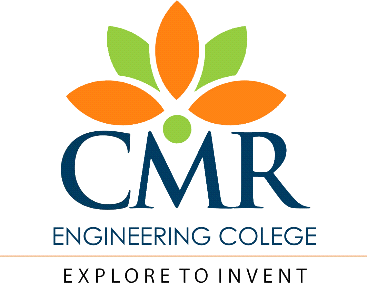
Computer Organization and Architecture

***Presented by :***

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Department of

**Computer Science and Engineering [AI&ML]**

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**CMR ENGINEERING COLLEGE**

(Approved by AICTE-New Delhi, Affiliated to J.N.T.U, Hyderabad)

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**(AY:2025-26)**

**ACADEMIC PLANNER**

**Computer Organization and Architecture**

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# PREAMBLE/INTRODUCTION

This course provides the basics of organizational and architectural issues of a digital computer analyze performance issues in processor and memory design of a digital computer. It also analyses various data transfer techniques in digital and performance improvement using instruction level parallelism. All students of computing should acquire some understanding and appreciation of a computer system’s functional components, their characteristics, their performance, and their interactions.

# PREREQUISITES

* 1. MM,M1, DATA STRUCTURES.

# OBJECTIVES AND OUTCOMES

## Course Objectives:

* The purpose of the course is to introduce principles of computer organization and the basic architectural concepts.
* It begins with basic organization, design, and programming of a simple digital computer and introduces simple register transfer language to specify various computer operations.
* Topics include computer arithmetic, instruction set design, micro programmed control unit, pipelining and vector processing, memory organization and I/O systems, and multiprocessors.

**Course Outcomes:**

|  |  |
| --- | --- |
| **CO1** | **Illustrate** the basics components and the design of the functional unit of digital computer system. |
| **CO2** | **Analyze** micro program instruction and make use of fixed and floating point algorithms. |
| **CO3** | **Describe** the fundamental data types and perform conversion between binary  - octal-hexadecimal – decimal representation. |
| **CO4** | **Develop** the memory hierarchy system ,cache memory , auxiliary memory. |
| **CO5** | **Implement** problem-solving skills by applying pipeline and vector processing techniques to optimize performance and efficiency in computing tasks. |

# SYLLABUS

### AUTONOMOUS-R22

**Computer Organization and Architecture**

B.Tech IIYear I SEM (R22)

Course Code: CS603PC

# UNIT - I

**Digital Computers**: Introduction, Block diagram of Digital Computer, Definition of Computer Organization, Computer Design and Computer Architecture.

**Register Transfer Language and Micro operations**: Register Transfer language, Register Transfer, Bus and memory transfers, Arithmetic Micro operations, logic micro operations, shift micro operations, Arithmetic logic shift unit.

**Basic Computer Organization and Design**: Instruction codes, Computer Registers Computer instructions, Timing and Control, Instruction cycle, Memory Reference Instructions, Input – Output and Interrupt.

### UNIT - II

**Micro programmed Control:** Control memory, Address sequencing, micro program example, design of control unit.

**Central Processing Unit:** General Register Organization, Instruction Formats, Addressing modes, Data Transfer and Manipulation, Program Control**.**

### UNIT – III

**Data Representation:** Data types, Complements, Fixed Point Representation, Floating Point Representation.

**Computer Arithmetic:** Addition and subtraction, multiplication Algorithms, Division Algorithms, Floating – point Arithmetic operations. Decimal Arithmetic unit, Decimal Arithmetic operations.

### UNIT – IV

**Input-Output Organization**: Input-Output Interface, Asynchronous data transfer, Modes of Transfer, Priority Interrupt Direct memory Access.

**Memory Organization:** Memory Hierarchy, Main Memory, Auxiliary memory, Associate Memory, Cache Memory.

### UNIT – V

**Reduced Instruction Set Computer**: CISC Characteristics, RISC Characteristics.

**Pipeline and Vector Processing:** Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processor.

**Multi Processors:** Characteristics of Multiprocessors, Interconnection Structures, Inter- processor arbitration, Inter-processor communication and synchronization, Cache Coherence.

### 1. GATE

Machine instructions and addressing modes. ALU, data-path and control unit. Instruction pipelining. Memory hierarchy cache main memory and secondary storage; I/O interface(interrupt and DMA mode).

# LIST OF EXPERT DETAILS

**The Expert Details which have been mentioned below are only a few of the eminent ones known Internationally, Nationally and Locally. There are a few others known as well.**

## International:

* **Name:** Edward Suh, Professor

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**Contact:** 519-888-4567 x31222

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**Contact:** 040-32408718

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**Contact:** 08724 229000.

# JOURNALS WITH MIN 5 REF PAPER FOR LITERATURE STUDY

* **TITLE :** Big Data Manipulation

**AUTHOR:** Syed Jamaluddin Ahmad, Roksana Khandoker Jolly

**LINK** : [file:///C:/Users/CSJAVA24/Downloads/DATA%20MANIPULATION.pdf](file://localhost/C:/Users/CSJAVA24/Downloads/DATA%20MANIPULATION.pdf)

* **TITLE :** Arithmetic of 5th Generation Computer

**AUTHOR:** Sinthia Roy1, Sanjit Kumar Setua2

**LINK:** [file:///C:/Users/CSJAVA24/Downloads/ARITHMETIC%20OPERATIONS.pdf](file://localhost/C:/Users/CSJAVA24/Downloads/ARITHMETIC%20OPERATIONS.pdf)

* **TITLE :** Comparative Study of RISC AND CISC Architectures

**AUTHOR:** Shahzeb1 , Naveed Hussain1, Abdul Wali Khan University Mardan,

**LINK:** [file:///C:/Users/CSJAVA24/Downloads/RISC%20VS%20CISC.pdf](file://localhost/C:/Users/CSJAVA24/Downloads/RISC%20VS%20CISC.pdf)

* **TITLE:** A Cycle-accurate Template Microprocessor Model of a Von Neumann Architecture Based on SystemC

**AUTHOR:** Lubomir Bogdanov, Ratcho Ivanov

**LINK:** [file:///C:/Users/CSJAVA24/Downloads/PIPELINING.pdf](file://localhost/C:/Users/CSJAVA24/Downloads/PIPELINING.pdf)

* **TITLE :** A REVIEW OF MEMORY ALLOCATION AND MANAGEMENT IN COMPUTER SYSTEMS

**AUTHOR:** AhmedFaraz

**LINK:** [file:///C:/Users/CSJAVA24/Downloads/MEMORY%20ALLOCATION.pdf](file://localhost/C:/Users/CSJAVA24/Downloads/MEMORY%20ALLOCATION.pdf)

# SUBJECT -LESSON PLAN

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **S. No** | **Topics/Sub topics covered** | **Lecture No** | **Text Book/ Reference Book** | **ICT Tools** |
| **UNIT I** | | | | |
| 1 | Introduction, Block diagram of Digital Computer | L1 | T1, T2 | M2 ,PPI |
| 2 | Definition of Computer Organization, Computer Design, Computer Architecture | L2 | T1, T2 | M1 |
| 3 | Register Transfer Language , Register Transfer | L3 | T1,R2 | M1 |
| 4 | Bus and Memory transfers | L4 | T1,R1 | M1 |
| 5 | Arithmetic Micro operations, Logic Micro Operations, Shift Micro Operations | L5-L7 | T1 | M2 ,PPT |
| 6 | Arithmetic Logic Shift Unit | L8 | T1,R2 | M2 ,PPT |
| 7 | Instruction codes, Computer Registers | L9 | T1 | M1 |
| 8 | Computer instructions. | L10 | T1 | M1 |
| 9 | Timing and Control, Instruction cycle | L11,L12 | T1, R3 | M2 ,PPT |
| 10 | Memory Reference Instructions | L13 | T1 | M2,PPT |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 11 | Input- Output and Interrupt | L14 | T1 | M1 |
| **UNIT II** | | | | |
| 12 | Design of control unit. | L15 | T1,R1,R2 | M2(PPT) |
| 13 | General Register Organization | L16 | T1 | M2(PPT) |
| 14 | Instruction Formats | L17 | T1 | M1 |
| 15 | Addressing modes | L18,L19 | T1,R2 | M2(PPT) |
| 16 | Data Transfer and Manipulation | L20,L21 | T1 | M1 |
| 17 | Program Control | L22 | T1 | M1 |
| **UNIT III** | | | | |
| 18 | Data types, Complements | L23 | T1 | M1 |
| 19 | Fixed Point Representation, Floating Point Representation. | L24,L25 | T1 | M1 |
| 20 | Addition and subtraction | L26,L27 | T1 | M1 |
| 21 | Multiplication Algorithms, Division Algorithms | L28,L29 | T1 | PPT,M2 |
| 22 | Floating – point Arithmetic operations | L30, L31 | T1 | M1 |
| **UNIT IV** | | | | |
| 23 | Input-Output Interface | L32 | T1 | M1 |
| 24 | Asynchronous data transfer | L33 | T1 | M1 |
| 25 | Modes of Transfer | L32,L33 | T1,R2 | M2(PPT) |
| 26 | Priority Interrupt Direct memory Access. | L34-L36 | T1,R3 | M2(PPT) |
| 27 | Memory Hierarchy, Main Memory | L37 | T1 | M2(PPT) |
| 28 | Auxiliary memory, Associate Memory  Cache Memory. | L38-L39 | T1 | M1 |
| **UNIT V** | | | | |
| 29 | CISC Characteristics, RISC Characteristics. | L40 | T1 | M2(PPT) |
| 30 | Parallel Processing, Pipelining | L41 | T1 | M2(PPT) |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 31 | Pipelining, Arithmetic Pipeline | L42 | T1 | M1 |
| 32 | Instruction Pipeline, RISC Pipeline | L43 | T1 | M2(PPT) |
| 33 | Vector Processing, Array Processor | L44 | T1 | M2(PPT) |
| 34 | Interconnection Structures | L45 | T1 | M2(PPT) |
| 35 | Inter processor arbitration | L46 | T1 | M2(PPT) |
| 36 | Inter processor communication and synchronization | L47 | T1 | M2(PPT) |
| 37 | Cache Coherence | L48 | T1 | M2(PPT) |

### METHODS OF TEACHING

|  |  |
| --- | --- |
| **M1 : Lecture Method** | **M6 : Tutorial** |
| **M2 : Demo Method** | **M7 : Assignment** |
| **M3 : Guest Lecture** | **M8 : Industry Visit** |
| **M4 : Presentation /PPT** | **M9 : Project Based** |
| **M5 : Lab/Practical /Activity** | **M10 : Charts / OHP** |

1. **SUGGESTED BOOKS (**prescribed and References)

### TEXT BOOKS:

**T1:** Computer System Architecture – M. Moris Mano, Third Edition, Pearson/PHI..

### REFERENCE BOOKS:

**R1:** Computer Organization – Car Hamacher, ZvonksVranesic, SafeaZaky, Vth Edition, McGraw Hill.

**R2:** Computer Organization and Architecture – William Stallings Sixth Edition, Pearson/PHI

**R3:** Structured Computer Organization – Andrew S. Tanenbaum, 4th Edition, PHI/Pearson

# WEBSITES FOR SELF LEARNING RESOURCES LIKE

* <https://nptel.ac.in/courses/106/105/106105163/>
* <https://www.coursera.org/learn/comparch>
* <https://www.javatpoint.com/computer-organization-and-architecture-tutorial>
* <https://www.geeksforgeeks.org/computer-organization-and-architecture-tutorials/>
* https://[www.tutorialspoint.com/differences-between-computer-architecture-and-computer-](http://www.tutorialspoint.com/differences-between-computer-architecture-and-computer-) organization

### QUESTION BANK:

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COA Question Papers.rar COA mid - 2 exam SET 2.rar COA mid - 1 exam SET 1.rar

# COMPUTER ORGANIZATION AND ARCHITECTURE

**UNIT WISE QUESTION BANK SHORT & LONG QUESTIONS**

**UNIT-I**

**SHORT QUESTIONS [2M**]

1. Define digital computer.
2. Write about memory read and memory write options.
3. Write short notes on three state buffers.
4. Explain the following.
   1. Register operand addressing mode
   2. Immediate operand addressing mode.
5. Write short notes on interrupt.
6. Write short notes on floating-point representation of decimal number.
7. What is the gray code equivalent of the Hex Number 3A7?
8. Differentiate cycle stealing and burst transfers of DMA.
9. What is the purpose of designing data communication processor?
10. What is vector processing?

### LONG QUESTIONS [10M]

1. Explain the components of the computer system.
2. What is a micro operation? Write about register transfer language.
3. What are register transfer logic languages? Explain few RTL statements for branching with their actual functioning.
4. Explain the following terms
   * Control word
   * Microinstructions
   * Micro program
   * Hardwired control
   * Pipeline register
   * Control address register
   * Control memory
   * Sequencer.
5. Describe how mapping from instruction code to microinstruction is done. Also, Explain about subroutines.
6. Explain Restoring Algorithm for Division with example.
7. Convert the following numbers.
   * 10101100111.0101 to Base 10
   * (153.513)10=()8
   * Given that (292)10 determine ‘b’.
8. Explain isolated IO vs. Memory mapped I/O.
9. Explain the strobe control method of asynchronous data transfer.
10. Discuss about Flynn’s classification of parallel processor systems.

### UNIT-II

**SHORT QUESTIONS [2M]**

1. Discuss in brief about microinstruction.
2. Draw a diagram that shows the register transfer implementation along with the timing diagram.
3. Distinguish between hardwired control unit and micro programmed control unit.
4. What are the three basic fields present in an instruction?
5. Find 9’s complement (25.639)10
6. Define fast multiplication circuit.
7. What is the purpose of designing data communication processor?
8. Compare between main memory and auxiliary memory.
9. Write a short note on cache coherence.
10. Discuss in brief about snooping protocol

### LONG QUESTIONS [10M]

1. Write about hardware implementation of the shift micro operations.
2. List and explain different types of computer instructions. Also provide their formats.
3. Give the comparison between zero-address, one-address, two-address and three- address.
4. Explain in detail about different addressing modes with example.
5. Explain in detail about floating point representation. Support your answers with Examples where required.
6. Explain how floating point numbers are represented? Represent the no. (+46.5)base 10 as a floating point binary number with 24 bits as 16 bits mantissa and 8 bits exponent.
7. Draw and explain the block diagram of RAM and ROM chips.
8. What are the different mapping techniques of cache memory? Describe each question with suitable diagram.
9. Discuss various dynamic arbitration techniques.
10. Explain in detail the following
    1. Inter processor communication
    2. Inter processor synchronization

### UNIT-III

**SHORT QUESTIONS [2M]**

1. Explain the instruction code format?
2. What do you mean by interrupt nesting?
3. List the four basic functions of the CPU?
4. Differentiate infix and post fix notations with an example?
5. What is an I/O channel?
6. State different ways to represent negative binary number?
7. What is pipeline scheduling?
8. Define cache hit, cache miss and hit ratio?
9. Discuss the principle behind the Booth's multiplier?
10. What do you mean by bus arbitration?

### LONG QUESTIONS [10M]

1. a) Give the block Diagram for Registers and Explain also discuss about memory Transfer Operations.
   1. Draw and explain the 4-bit combi-national shifter circuit.

### OR

1. a) Draw and explain the input-output configuration for basic computer.
   1. Discuss the basic structure of micro program control unit.
2. Illustrate Address sequencing with neat block diagram.

### OR

1. a) With a neat diagram, explain address selection for control memory.
   1. Explain how X=(A+B)/(A-B) is evaluated in a stack based computer.
2. a)Explain micro program sequencer with block diagram.

### OR

b) Why do we need subroutine register in a control unit? Explain.

1. a) Write a program to evaluate the arithmetic statement Y= (A+ B)\* (C+D) using

a. Three-address, two-address, one-address and zero-address instructions.

### OR

1. a) Explain various addressing modes with example.

### OR

b).Draw and explain the overflow detector logic circuit for integer addition .

1. a) Draw and explain the block diagram of typical DMA controller.
2. a)Explain various cache mapping techniques.

### OR

* 1. Explain data hazards in detail.

20. Explain the inter processor communication using shared variables.

### UNIT-IV

**SHORT QUESTIONS [2M]**

1. Define computer architecture?
2. Give the classification of micro-operations used in the digital system.
3. What is address sequencing?
4. List and example types of Interrupts ?
5. Convert (5632.471)8 to decimal number and explain the process of conversion ?
6. What is fixed point number System ?
7. What is function of I/O interface?
8. How many address bits are needed to operate a 2K\*8 ROM?
9. What is risk?
10. What is vector processor?

### LONG QUESTIONS [10M]

1. a) List the four basic functions of the CPU?
   1. Draw and explain the hardware to implement integer addition and subtraction.

### OR

1. a)Discuss various registers along with their purpose?
   1. List various memory reference instructions with their functionality?
2. a) discuss the basic structure of micro program control unit.
   1. With a neat diagram, explain Design of control unit for decoding Micro operations.

### OR

1. a) What is instruction format and explain micro instruction format.
   1. Write a program to evaluate the arithmetic statement Y=(a+b)\*(c+d) using three- address, two-address, one-address and zero-address.
2. .Explain Hardware Implementation of Signed Magnitude Addition and Subtraction?

### OR

1. a) What is meant by data types and explain floating point representation with examples.

b) Explain booth's multiplication algorithm for multiplying binary integers in signed 2's compliment representation.

1. a) Explain I/O interface.
   1. Explain DMA.

### OR

1. Explain memory hierarchy in detail.
2. a) Explain the characteristics of CISC architecture.
   1. Explain the pipeline for floating point addition and subtraction.

### OR

12. a) What is an array processor? Explain the different types.

b) Give the comparison between CISC and loosely RISC systems.

### UNIT-V

**SHORT QUESTIONS [2M]**

1. Write about decode phase of instruction cycle.
2. Write about timing signal.
3. List any two differences between one-address and three address instructions.
4. Discuss about internal interrupts.
5. Write short notes on underflow.
6. Write short notes on overflows.
7. What do you mean by associative memory?
8. List the characteristics of memory devices.
9. What is vector processing?
10. Give the instruction format for vector processor.

### LONG QUESTIONS [10M]

1. List and explain different types of computer instructions. Also provide their formats.
2. Explain how the computer provides control and timing

### OR

Explain the organization of control unit of basic computer.

1. Tabulate various data transfer and manipulation instructions.
2. Discuss in brief about program control instructions.
3. What is overflow and underflow? What is the reason? If the computer is considered as infinite system, do we still have these problems?
4. Draw a flowchart to explain how addition and subtraction of two fixed point numbers can be done. Also, draw a circuit using full adders for the same.
5. Draw and explain the block diagram of RAM and ROM chips.
6. What are the different mapping techniques of cache memory? Describe each question with suitable diagram.
7. What is meant by instruction pipeline? Explain four segment instruction pipeline.
8. Give the timing diagram of instruction pipeline.

# TWO CASE STUDY PRESENTATIONS WITH PROJECT / PRODUCT/ MODEL /PROTOTYPES/ INDUSTRIAL APPLICATIONS. CASE STUDY:

**Case Study 1: The Slow Game Loading Issue**

* **Scenario:** Your friend, a passionate gamer, is constantly frustrated because their favorite open-world game takes an incredibly long time to load. They have a decent graphics card and a good internet connection, but the loading screens seem to last forever, often making them miss the start of online matches.
* **Problem:** The game loads very slowly, even though other components seem fine.
* **Computer Organization & Architecture Connection:**
  + **Memory Hierarchy (RAM and Storage):** The most likely culprit here is the storage device. Games, especially open-world ones, have massive amounts of data (textures, models, audio) that need to be loaded into the computer's RAM.
    - If your friend is still using a traditional **Hard Disk Drive (HDD)**, it has spinning platters and read/write heads, which are much slower at accessing data compared to solid-state drives.
    - **Solid State Drives (SSDs)**, on the other hand, use flash memory and have no moving parts, leading to significantly faster data access.
  + **Bus Speed:** While less likely to be the primary cause here, the speed at which data travels between the storage device, the CPU, and RAM (via the system bus) also plays a role. A slower bus can create a bottleneck.
* **Solution & Outcome:** You suggest to your friend that they upgrade their computer's storage from an HDD to an **SSD**. After installing the SSD and reinstalling the game, the loading times are dramatically reduced. They can now join online matches promptly and enjoy a much smoother gaming experience. This demonstrates how a faster storage device, a key component in the memory hierarchy, directly impacts performance in data-intensive applications.

**Case Study 2: The Stuttering Video Editing Project**

* **Scenario:** Your cousin is trying to edit a high-definition video for a school project. They've imported all the clips, but when they try to play back the timeline or apply even simple effects, the video stutters, freezes, and the editing software becomes unresponsive. They've tried restarting the computer, but the problem persists.
* **Problem:** The video editing software is performing very poorly, making it impossible to edit the video smoothly.
* **Computer Organization & Architecture Connection:**
  + **CPU (Central Processing Unit):** Video editing is a computationally intensive task. It involves decoding video frames, applying filters, rendering effects, and encoding the final output. A weak or old CPU might struggle to keep up with these demands, leading to stuttering and unresponsiveness.
  + **RAM (Random Access Memory):** Video editing software often needs to hold many frames and processing instructions in RAM to work efficiently. If the computer has insufficient RAM, it will constantly have to swap data to slower storage (like the hard drive), causing significant slowdowns.
  + **Cache Memory:** While often overlooked, the CPU's small, fast cache memory helps store frequently accessed data. If the cache is too small or inefficient, the CPU has to fetch data from slower RAM more often, impacting performance.
* **Solution & Outcome:** You examine your cousin's computer specifications and notice they have an older CPU and only 4GB of RAM. You advise them to upgrade their RAM to at least 16GB and, if possible, consider a CPU upgrade. After upgrading the RAM, the video editing software performs much better. The video plays back smoothly, and they can apply effects without significant delays. This highlights the crucial role of adequate CPU power and sufficient RAM in handling demanding computational tasks like video editing

# ASSIGNMENT QUESTIONS

### SET I

* 1. Explain block diagram of digital computer?
  2. Explain instruction codes for stored program organization
  3. List out register Reference instructions?
  4. Draw and explain flow chart of basic computer

### SET II

1. Explain Basic computer instructions with examples
2. Draw and explain Block diagram of control unit of basic computer?
3. List out memory reference instructions?

### SET III

1. Draw the flow chart of instruction cycle and explain steps involved in instruction cycle?
2. Explain memory reference instructions with flow chart?
3. Explain interrupt cycle with flow chart?
4. Explain Program counter?

### SET IV

1. Explain micro programmed control unit?
2. How to select address of next instruction explain with flow chart?
3. Explain Basic computer instruction format?
4. List out register Reference instructions?.

### INNOVATIVE ASSIGNMENTS SETS.

* Design Your Own CPU (Mini Project-Based)
* Analyze and Compare: RISC vs. CISC Architectures.
* Cache Mapping Strategy Simulation.
* Instruction Cycle Visualization
* Energy-Efficient CPU Design (Research-Based)

### LIST OF TOPICS FOR STUDENTS SEMINARS WITH GUIDELINES.

* Design of Control Unit
* Bus Structure
* Direct Memory Access
* Modes of Transfer
* Instruction cycle

### STEP/COURSE MATERIAL IN SOFTCOPY.

COA .RAR.zip

COA.zip

### EXPERT LECTURES WITH TOPICS & SCHEDULES (IF ANY)

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1. **ACTIVITY PLAN**

**Week wise Activity plan**

|  |  |  |
| --- | --- | --- |
| **S.no** | **week** | **Activity** |
| 1 | 1 | **Topic** wise test question will give to the students |
| 2 | 2 | **Seminar** and topic wise question will give to the students |
| 3 | 3 | **Snap Talk** and topic wise question will give to the students |
| 4 | 4 | **Assignments** and topic wise question will give to the students |
| 5 | 5 | **One minute** question on subject |
| 6 | 6 | **Group Discussion** On Topic Wise Question Will Give To The Students |
| 7 | 7 | **Draw architecture** and block diagram topic wise |
| 8 | 8 | **Role Play** and topic wise question will give to the students |
| 9 | 9 | **Topic wise test** question will give to the students |
| 10 | 10 | **Quiz** sessions and topic wise question will give to the students |